A hybrid clock tree with multi-spine using automated design methodology for low cost and low power complex LSIs

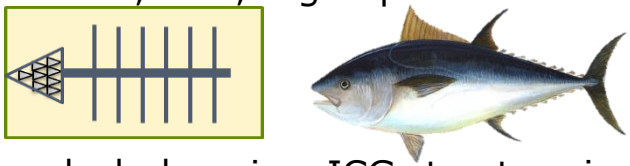
Takashi Hasegawa, Maki Yajima, Makoto Fujiwara, Takanori Saeki
Sony LSI Design Inc., Kanagawa, Japan.

Introduction

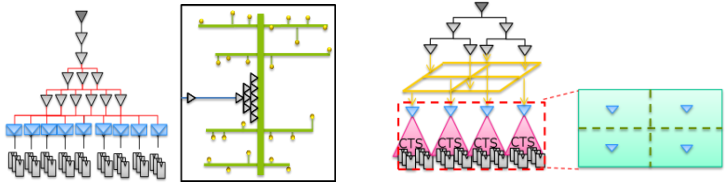
- Several clock distribution concepts have been proposed.
- Categorize them from design points of view, as below.

Tuna type

MPU, NoC, High Speed IF ・・・



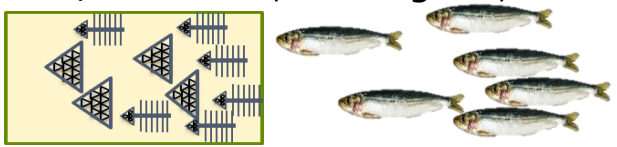
A few clock domains, ICG structure is simple



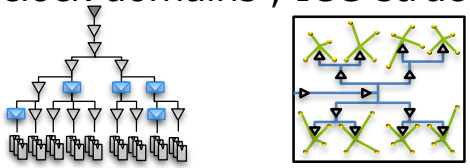
Traditional Mesh(grid)/Fishbone(Spine) , Hybrid Clock

Sardines type

Low power/cost SoCs, Mix-Signal , IoTs ・・・



Many clock domains , ICG structure is complex



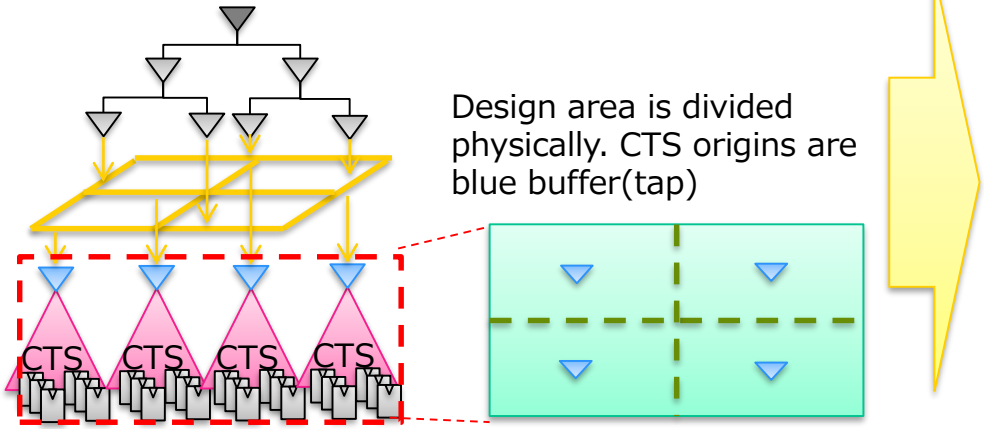
CTS

- Conventional concepts for “tuna” designs is costly and unsuitable for “sardines”
- Most of our commercial chips are categorized into “sardines” designs.
- The quality of CTS is not enough.
- **The new concept of lower power and less effort is required.**

Motivation

- The conventional hybrid clock tree is not suitable for “sardines” designs (low cost and low power complex LSIs.)

■Conventional Hybrid Clock Tree

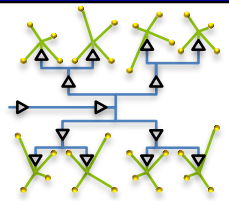
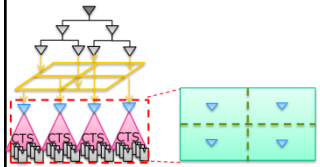
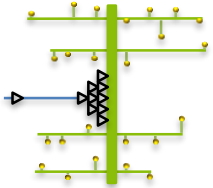
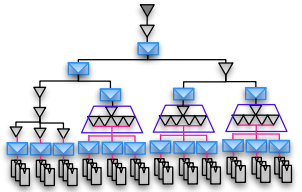


Design area is divided physically. CTS origins are blue buffer(tap)

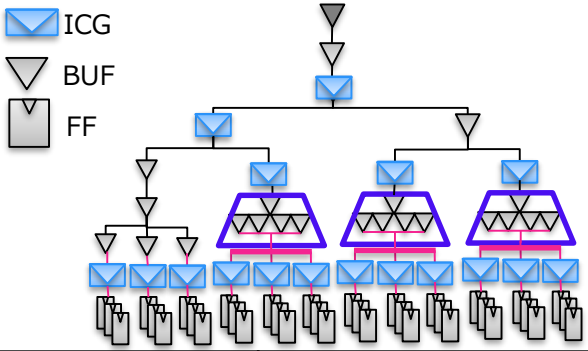
- Our common design characteristics
  - Middle sized designs (<5M instances)
  - Many clock domains (50+)
  - Fewer layers (use only IM layers)
  - Complicated clock gating(ICG) structure
  - Not high speed (several hundreds of MHz)
- **A conventional concept is not effective due to the limitation of size and ICG structure.**
- Our design requires low power and short TAT.

- A proposed clock distribution concept and design methodology,
  - Much lower power as well as better quality.
  - Automated method with custom cells reduces engineering time drastically.

Comparison with conventional concepts

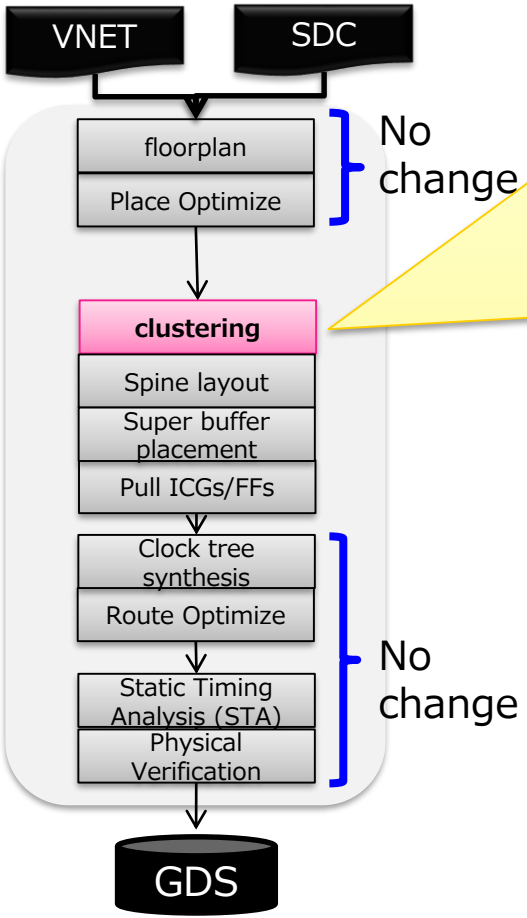
		CTS by commercial tools	Conventional Hybrid Clock	Conventional Spine	**Proposed Hybrid clock**
	Layout image				
Application		**“Sardines Type”** (Mix-Signal Low-power/cost SoC)	“Tuna Type” (MPU, NoC, High Speed IF)	“Tuna Type” (MPU, NoC, High Speed IF)	**“Sardines Type”** (Mix-Signal Low-power/cost SoC)
Target Design	Size	Any	Large designs	Large designs	**Any**
	Speed	Under GHz	Over GHz	Over GHz	**Under GHz**
	structure	Any	simple	very simple	**Any**
	Layer number	Any	Need thick metal	Need thick metal	**Any**
Result	effort	Minimum	A lot	A lot	**Minimum**
	skew	Not good	Good	Very good	**Good**
	power	Not good	Not good	Good	**Good**

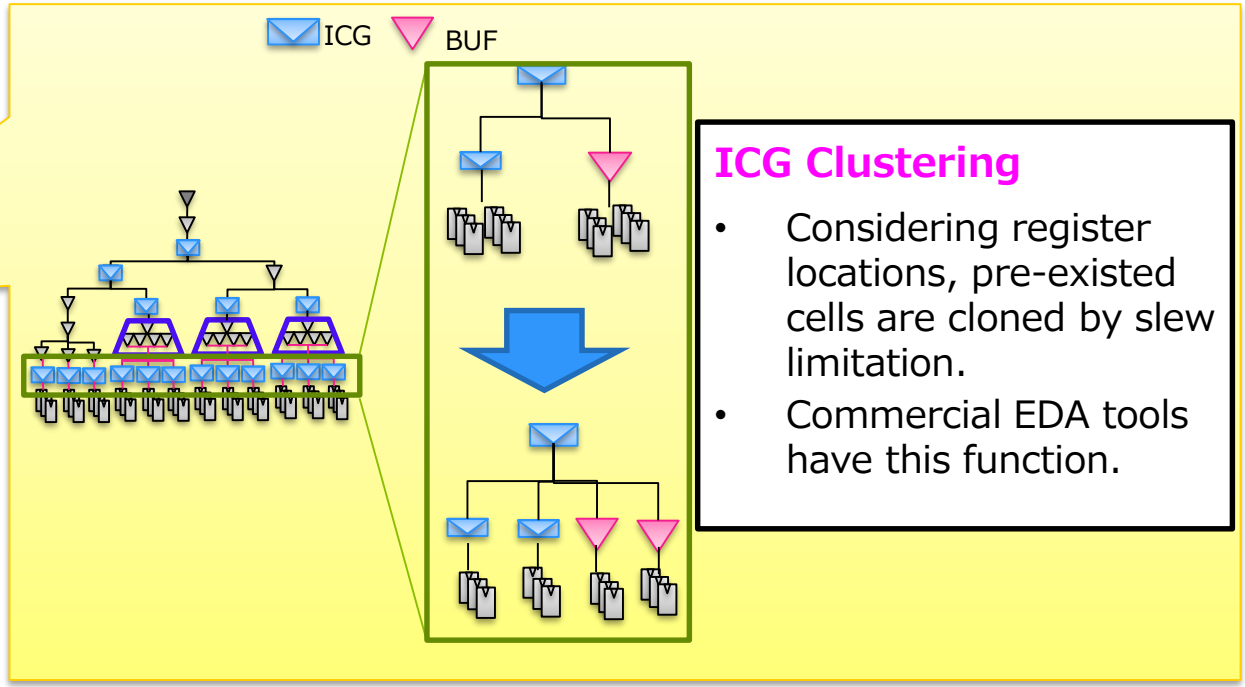
Proposed concept : “hybrid clock tree-spine”

	Proposed concept “Hybrid clock tree-spine”	
		
Target Design	Size	**Any**
	Speed	**Under GHz**
	structure	**Any**
	Layer number	**Any**
Result	effort	**Minimum**
	skew	**Good**
	power	**Good**

- **Global CTS and multi-spine structures.**
  - Global CTS can handle any size , structure.
  - Multi small spines doesn’t need thick metal
- **Optimized super buffers**
  - STA is able to be used
- **Optimized spine layout**
  - Lower power than CTS.
  - Better skew than CTS.
- **Required to be same effort as CTS.**
  - Need automated methodology

Design methodology: ICG Clustering

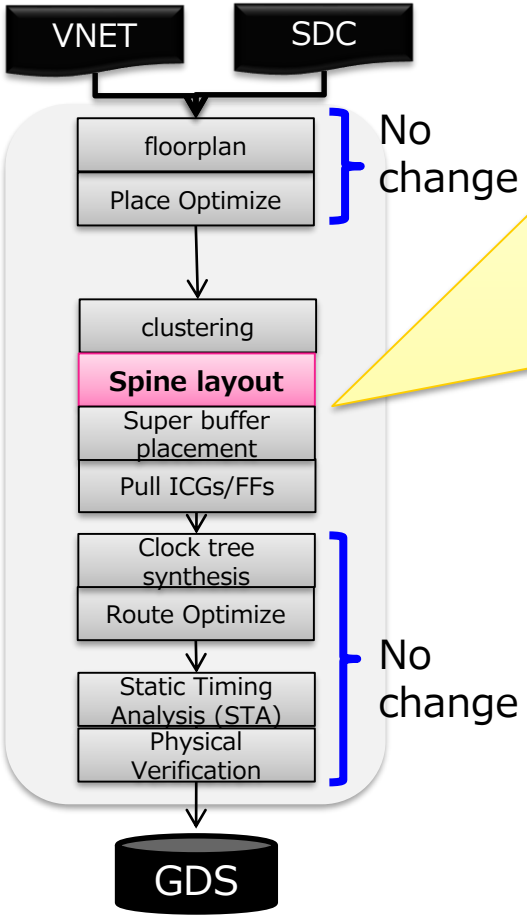


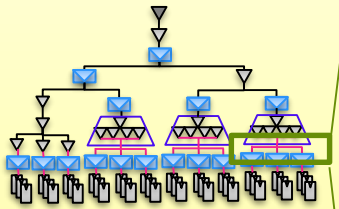


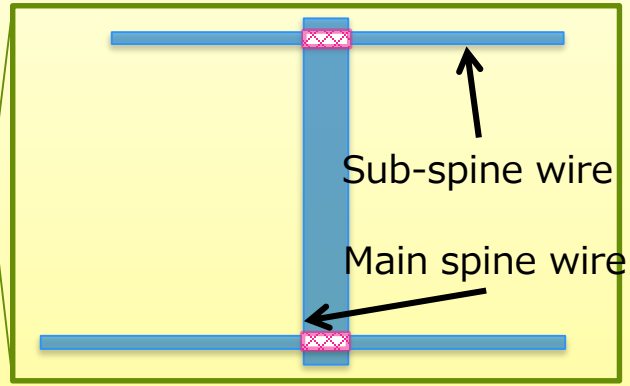
ICG Clustering

- Considering register locations, pre-existed cells are cloned by slew limitation.
- Commercial EDA tools have this function.

Design methodology: Spine wire-width optimizing



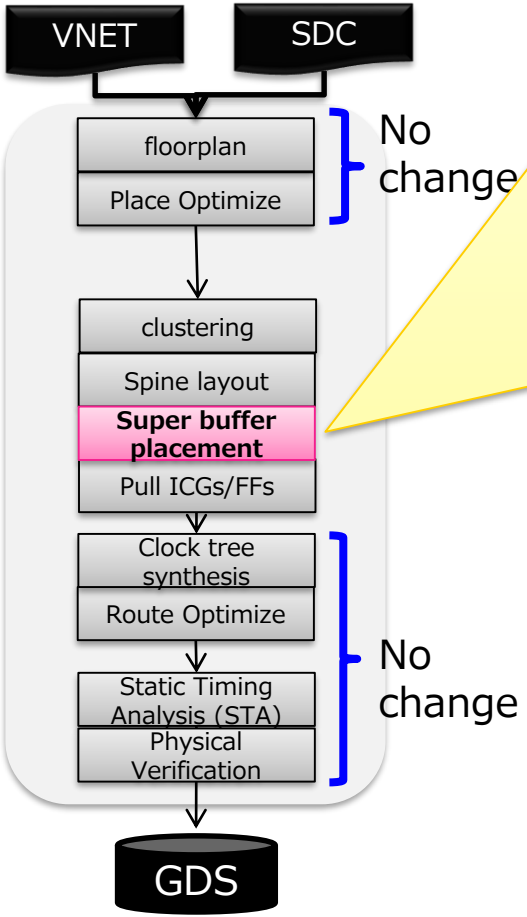


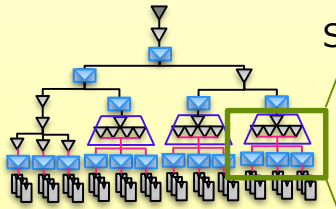


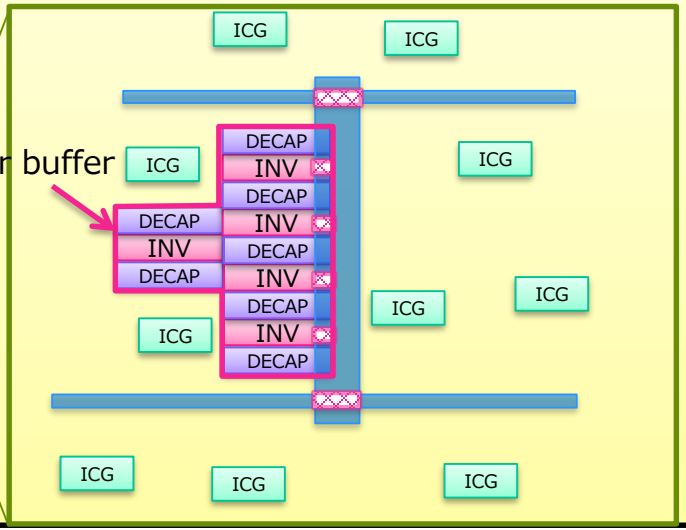
Spine wire-width optimizing

- Spine wires should be narrower for lower power.
  - Spine Wire Width = max (min width by EM criteria , min width by slew criteria)
- In-house Script automatically generates the spine layout.

Design methodology: Super buffer for optimized spines



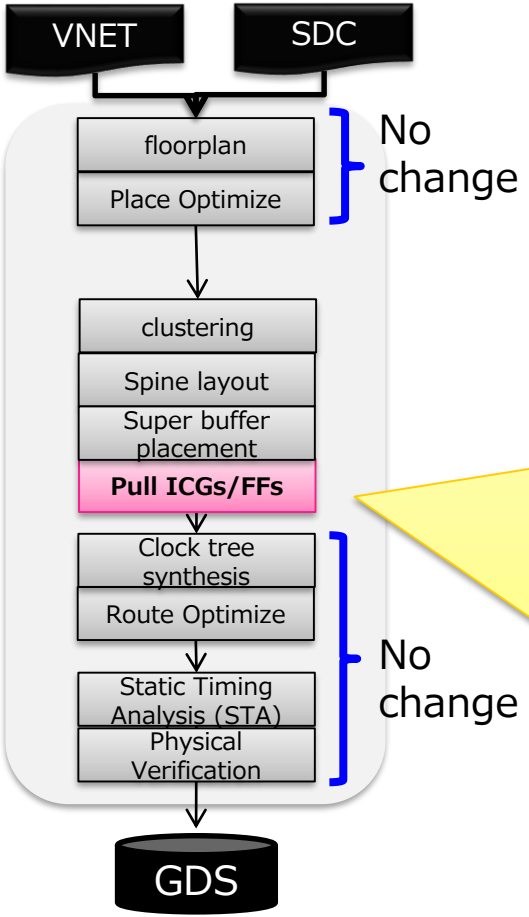


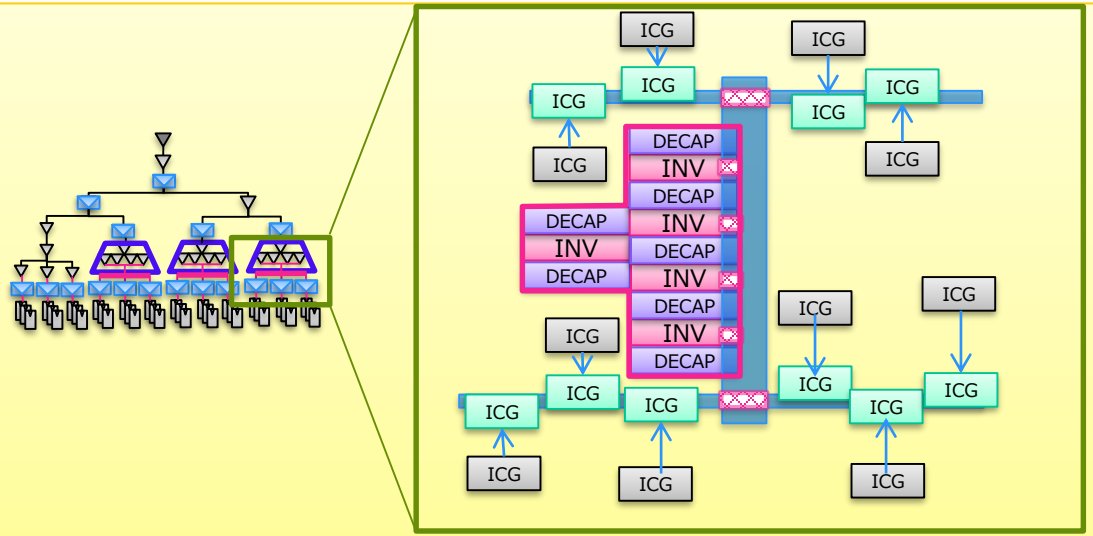


Super buffer for optimized spines

- The driving strength of super-buffers is decided by the slew criteria.
- Key Features of customized super-buffers
  - Wide-range buffer-sizing variations (x50～ x1600).
  - Transistors in cells are placed carefully to consider noise.
- In-house Script automatically calculate cell-size and pre-place.

Design methodology: ICGs placement optimization





ICGs placement optimization

- ICGs are relocated under sub-spine wire for reducing clock power before ICGs.
- In-house Scripts automatically move and optimize them.

This flow can reduce engineering time drastically compared with conventional one.

Application designs

- Applied proposed “Hybrid clock tree-spine” into our 3 industrial designs.

	Design information					
name	**Process**	**# of Instance**	**# of Clock domain**	**Clock gating level**	**# of FF bits**	**Frequency**
Design A	40nm 6Cu	1.9M	45	4	380K	200MHz
Design B	40nm 6Cu	2.1M	62	5	360K	230MHz
Design C	40nm 6Cu	1.7M	62	5	360K	230MHz

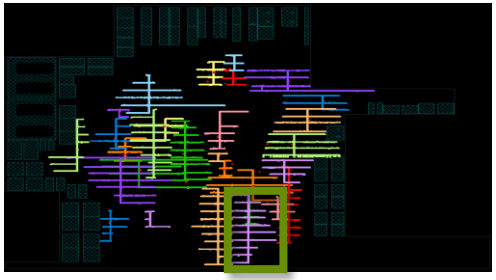
- Design A
  - Compared with a full CTS result, under same netlist and same locations of registers on CAD tool.
- Design B and C
  - RTL2GDS comparison (same RTL). Compared on Si as well as CAD tool.

A Detail Result of design “A”

The result of the comparison between CTS and “hybrid clock tree-spine” on one clock domain.

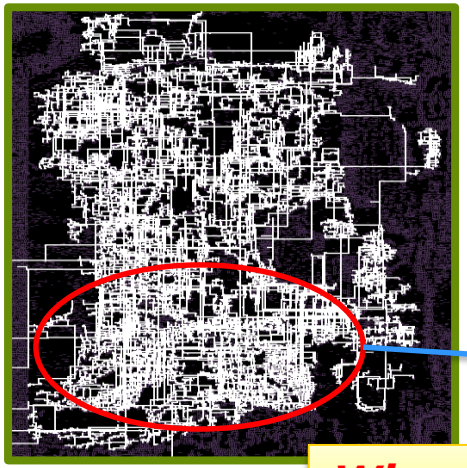
■ Design A
- S/C instances : 1.9M
- clock domains : 45
- process/layer : 40nm 6Cu (5 thin layer)

Locations of registers are same.



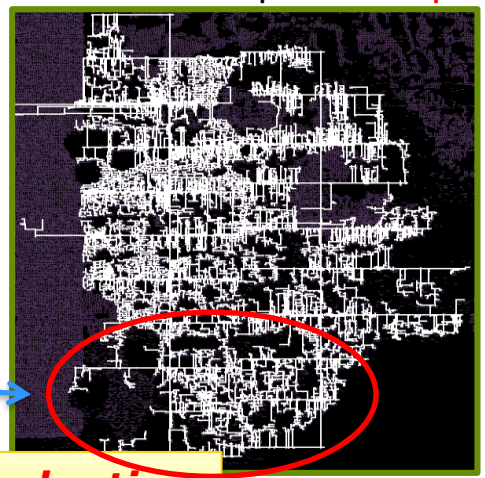
◆Full low-power CTS by commercial tools
ClockWire Cap : 25pF

◆Hybrid clock tree-spine (proposed)
ClockWire Cap : 16pF



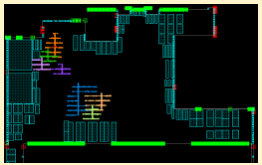
Highlighted wire from root to sink points

The wire length is apparently improved.



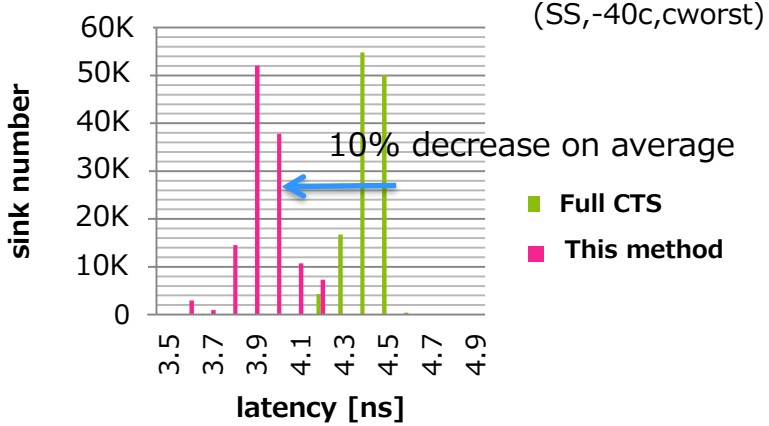
Wire Capacitance 37% Reduction

An implementation Result

	Design Layout 40nm 6Cu (5 thin layer)	Clock Power result (TT,25c,rctypical)	
	Layout view	Full CTS (commercial tool)	Hybrid clock tree-spine
Design A ※registers' locations are same.		24mW → **21mW** **15%** reduction	
Design B		58mW → **42mW** **27%** reduction	
Design C		50mW → **36mW** **28%** reduction	

	Design A case		Tuna design (reference)
	Full CTS (commercial tool)	Hybrid clock tree-spine	Conventional hybrid clock
Engineer Time	1 week	**1.5 week**	12 weeks

■The main clock skew/latency histogram (design A) (SS,-40c,cworst)



- **"Hybrid cock tree-spine" is proven in Si** at design B and C.
  - Total power reduction: 15% at CAD tool, 13% at Si. Their yields are same.

Result and Summary

- We proposed hybrid clock tree-spine and the automated design methodology for “sardines” designs (low cost and low power complex LSIs).

- Comparing with a full CTS at “sardines” designs.

  - Custom cells and an in-house automated flow achieve **almost same productivity and engineer time.**
  - 37% capacitance reduction of clock wire in one domain due to optimized spine layout and ICG placement.
  - **15-28% power reduction of all clock networks**, 10% reduction of clock latency from PLL and 50% hold TNS reduction enjoying the benefit of the spine based clock.

- **These results were proven in Si**. A ratio of power reduction was almost same as we expected on EDA tool.